

# Methods for Measurement and Simulation of Weak Substrate Coupling in High-Speed Bipolar ICs

Wolfgang Steiner, Martin Pfost, *Member, IEEE*, Hans-Martin Rein, *Fellow, IEEE*, Anton Stürmer, and Andreas Schüppen

**Abstract**—On-wafer measurements of very weak substrate coupling in high-speed integrated circuits (ICs) at high frequencies suffer from the direct crosstalk between the input and output RF probes. Two alternative methods to reduce this effect are presented and compared. The first one is based on an advanced deembedding method that eliminates the crosstalk between the RF probes after measurement. The second method utilizes an on-chip broad-band amplifier between the input probe and the substrate test structure. Thus, for a given signal amplitude at the output probe, the amplitude of the input signal can be reduced, resulting in less distortion of the output signal by the crosstalk via the probes. Both methods are compared and verified by measurements up to about 20 GHz even at substrate coupling impedances as high as  $0.5 \text{ M}\Omega$  (corresponding to  $-80 \text{ dB}$  in a  $50\text{-}\Omega$  system). For this, several substrate test structures (some with the 20-GHz on-chip amplifier) have been designed and fabricated in an SiGe bipolar production technology with  $20\text{-}\Omega\text{cm}$  substrate resistivity. The measurement results agree well with simulation results using our substrate simulator SUSI. As a consequence, the inflexible, expensive, and time-consuming way to determine substrate coupling experimentally is no longer required in future IC designs—not even at very weak coupling and high frequencies. In this work, however, the proposed measuring methods had to be applied to verify the suitability of substrate simulation (with SUSI) under extreme conditions.

**Index Terms**—On-wafer measurement techniques, substrate coupling, substrate coupling simulation.

## I. INTRODUCTION

WITH increasing operation frequencies of today's high-speed integrated circuits (ICs), degradation of circuit performance by substrate coupling is of growing influence. Typical examples are mixed-mode and high-gain analog ICs. Especially critical are amplifier arrays for parallel optical transmission links with small distances on the chip. To avoid redesigns, it is necessary to consider the effects of the substrate on circuit performance by careful simulation.

There are several recent publications that focus on the simulation and measurement of substrate coupling [1]–[13]. However, most of them are restricted to ICs operating at lower frequencies (around and below 1 GHz), therefore, neglecting the dielectric

Manuscript received February 22, 2001. This work was supported by the German Bundesministerium für Bildung und Forschung under Contract 01M3037 C.

W. Steiner and H.-M. Rein are with the Ruhr-University Bochum, D-44780 Bochum, Germany.

M. Pfost was with the Ruhr-University Bochum, D-44780 Bochum, Germany. He is now with Infineon Technologies, WS TI S G3, D-81739 Munich, Germany.

A. Stürmer is with Atmel Germany, IT13, D-89081 Ulm, Germany.

A. Schüppen is with Atmel Germany, D-74025 Heilbronn, Germany.

Publisher Item Identifier 10.1109/TMTT.2002.800392.

behavior of the substrate. This simplification does not hold for high-speed Si bipolar ICs because of the relatively high resistivity of the substrate (typically  $10\text{--}20 \text{ }\Omega\text{cm}$ ) commonly used in such circuits. Moreover, at very high frequencies, the parasitic inductance of metallization layers, especially in the case of shielding, requires careful attention as well.

To the best of the authors' knowledge, only a few publications contain both measurements and simulations up to about 10 GHz [11] and above [12]. The simulations in [11] and [12] were performed by use of the device simulator MEDICI and are restricted to two-dimensional (2-D) configurations. In practice, a simulator is required which can calculate three-dimensional (3-D) problems within a reasonable computing time.

To address this need, the numerical substrate simulator SUSI has been developed with main focus on high-speed bipolar ICs. This simulator (described in [14] and [15]) uses the technique of finite boxes as its discretization method and allows automatic generation and refinement of the simulation grid, based on the distribution of the electrical potential within the regions under investigation. It not only models the substrate region including its dielectric behavior (required at high frequencies), but also the other regions on the chip that tend to have a strong influence on substrate coupling as channel stopper and inversion layers, as well as on-chip metallization, and oxide layers.

The accuracy of the simulator SUSI has already been verified by on-chip measurements up to 40 GHz, but not under extreme conditions. The experimental verification of SUSI for very weak substrate coupling at high frequencies (here down to  $-80 \text{ dB}$  at 10 GHz) is, therefore, the main topic of this paper. A sufficient agreement between simulation and measurement would predestine SUSI as a powerful tool also to investigate shielding methods in high-frequency ICs.

A main problem of on-wafer measurements of very weak substrate coupling is the crosstalk between the input and output RF probes, which can lead to severe measurement errors and, therefore, must be taken into account. In this paper, two methods are discussed which proved to be well suited to reduce the influence of probe crosstalk. To the best of the authors' knowledge, both methods have not yet been discussed in the literature. The first one, described in Section II, is an advanced deembedding method which requires additional measurements and allows us to eliminate the crosstalk numerically. The second one, presented in Section III, utilizes a broad-band amplifier which amplifies the input signal on-chip and thus reduces the required input signal level. As a consequence, the parasitic signal coupled from the input to the output probe is substantially reduced. Both methods are compared in Section IV, followed by

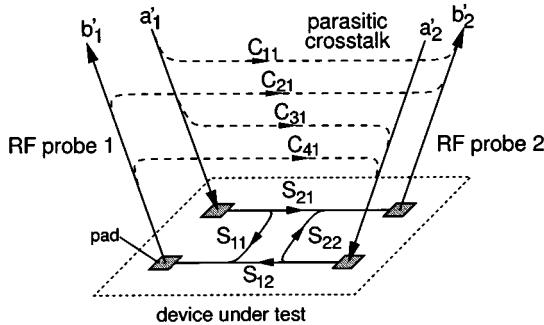


Fig. 1. Model used to describe the crosstalk between the RF probes. The crosstalk paths from probe 1 to probe 2, modeled by  $C_{11}$ ,  $C_{21}$ ,  $C_{31}$ , and  $C_{41}$ , are depicted here as dashed lines. The other direction is handled similarly (not shown).

a description of the substrate test structures under investigation in Section V. Finally, in Section VI, measurement results are presented and compared with simulation results obtained with SUSI. Moreover, the effectiveness of different shielding measures is discussed.

## II. DEEMBEDDING OF CROSSTALK BETWEEN THE RF PROBES

In the following discussion, we will assume that the vector network analyzer used for the measurements has already been calibrated with a seven-term method such as TRL or LRM [16]. In that case, only the crosstalk between the two RF probes has to be taken into account, which can be considered by the simple error model shown in Fig. 1.<sup>1</sup> It uses four coefficients  $C_{11}$ ,  $C_{21}$ ,  $C_{31}$ ,  $C_{41}$  to model the crosstalk from probe 1 to probe 2. Similarly, the other direction is modeled by  $C_{12}$ ,  $C_{22}$ ,  $C_{32}$ , and  $C_{42}$  (not shown). The test structure under investigation is described by the scattering parameters  $S_{11}$ ,  $S_{12}$ ,  $S_{21}$ , and  $S_{22}$ , while the quantities  $a'_1$ ,  $b'_1$ ,  $a'_2$ , and  $b'_2$  denote the waves measured by the network analyzer. (The apostrophes indicate that these quantities are affected by crosstalk.)

Using this model, we obtain

$$b'_2 = (S_{21} + C_{11} + C_{21}S_{11} + C_{31}S_{22} + C_{41}S_{11}S_{22})a'_1 + S_{22}a'_2 \quad (1)$$

$$b'_1 = (S_{12} + C_{12} + C_{22}S_{11} + C_{32}S_{22} + C_{42}S_{11}S_{22})a'_2 + S_{11}a'_1. \quad (2)$$

An important observation for typical on-wafer setups is that the measurement error of the *reflections* (i.e.,  $S_{11}$  and  $S_{22}$ ) is significantly higher than the crosstalk via the RF probes (in our case:  $-50$  dB versus  $-70$  dB, respectively, at 10 GHz). Thus, it is reasonable to neglect the influence of the crosstalk on the reflections, leading to

$$S_{11} = \left. \frac{b'_1}{a'_1} \right|_{a'_2=0} \quad \text{and} \quad S_{22} = \left. \frac{b'_2}{a'_2} \right|_{a'_1=0}. \quad (3)$$

<sup>1</sup>Strictly speaking, the crosstalk of the whole measurement setup is modeled. However, the contribution of the RF probes is the dominating one.

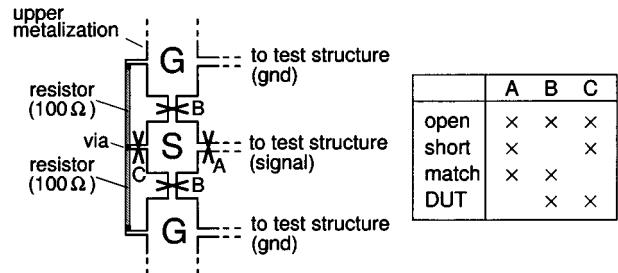


Fig. 2. Pad configuration for a ground-signal-ground (GSG) RF probe. By cutting interconnections at the positions denoted by A, B, and C as shown in the table, the standards “open,” “short,” and “match” can be realized and the test structure for substrate coupling (DUT) can be activated.

With the transmissions measured by the network analyzer, defined as

$$S'_{21} = \left. \frac{b'_2}{a'_1} \right|_{a'_2=0} \quad \text{and} \quad S'_{12} = \left. \frac{b'_1}{a'_2} \right|_{a'_1=0} \quad (4)$$

we get

$$S'_{21} = S_{21} + C_{11} + C_{21}S_{11} + C_{31}S_{22} + C_{41}S_{11}S_{22} \quad (5)$$

$$S'_{12} = S_{12} + C_{12} + C_{22}S_{11} + C_{32}S_{22} + C_{42}S_{11}S_{22}. \quad (6)$$

To obtain the transmissions  $S_{21}$  and  $S_{12}$  of the test structure only, the crosstalk of the probes has to be eliminated. For this, the coefficients  $C_{\nu 1}$  and  $C_{\nu 2}$  ( $\nu = 1, \dots, 4$ ) are required, which can easily be calculated from (5) and (6) by measuring four different standards with known reflections and transmissions.

An important prerequisite for this is that the coefficients  $C_{\nu 1}$  and  $C_{\nu 2}$  remain constant for all measurements. Consequently, the spacing between the RF probes must not be altered. Moreover, since the metallization of the test structure also has an influence on the total crosstalk, it is necessary that the metallization of the standards is as similar as possible to that of the test structure. This can be accomplished by extending the contact pad configuration used for the RF probes as shown in Fig. 2. Thus, the commonly used standards “open,” “short,” and “match” (which are not required to be ideal) can easily be realized by cutting the appropriate connections using an ultrasonic cutter. Their reflections  $S_{11}$  and  $S_{22}$  are obtained by measurements, while their transmissions  $S_{21}$  and  $S_{12}$  are assumed to be zero because the connections “A” are cut.

The reflections ( $S_{11}$  and  $S_{22}$ ) of the substrate configurations investigated here have a magnitude close to unity. Consequently, for obtaining the most accurate results the coefficients  $C_{\nu 1}$  and  $C_{\nu 2}$  of the deembedding procedure are preferably determined using standards with similarly high reflections. In this case, the combinations of the open and short standards were used, i.e., open/open, open/short, short/open, and short/short (related to the input/output port).

Other possible combinations of the standards can be applied to check the accuracy of the deembedding procedure. As an example, the standards match/match and match/open are used at the input/output port. Fig. 3 shows the uncorrected and corrected transmissions  $S'_{21}$  and  $S_{21}$ , respectively, for these configurations. It can be observed that the deembedding method reduces

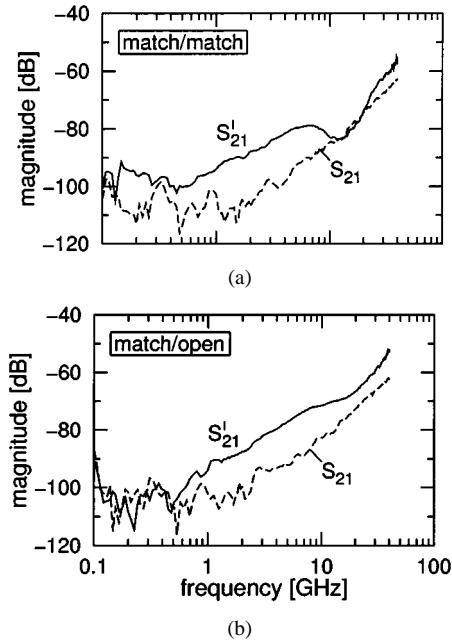


Fig. 3. Verification of the deembedding procedure using the standards: (a) match/match and (b) match/open. Shown are the magnitudes of the transmissions  $S'_{21}$  and  $S_{21}$ , without and with correction, respectively.

the transmission substantially in both cases, even considering the fact that the match has a reflection quite different from the open and short standards used for calculating the deembedding coefficients. Based on these results, it can be expected that the influence of RF probe crosstalk, which is of interest for measurements of very weak substrate coupling, is reduced by about 10–20 dB applying the proposed method.

### III. ON-CHIP BROAD-BAND AMPLIFIER FOR REDUCING CROSSTALK BETWEEN THE RF PROBES

#### A. Measuring Principle

As another possibility to reduce the influence of crosstalk between the RF probes on the measurement results, the substrate test structure can be driven by a broad-band amplifier located on the same chip. For a given signal amplitude at the output probe, the amplitude at the input probe can be reduced according to the amplifier's gain, thus reducing the noise coupled from the input to the output probe.

Fig. 4 shows the measuring setup and the amplifier/test-structure configuration including the probe pads. For the amplifier, a differential configuration is used (cf. Section III-B), and its layout is symmetrical to the axis between input ( $I - \bar{I}$ ) and output ( $Q - \bar{Q}$ ). These measures reduce the noise in the substrate and on the supply lines generated by the amplifier as well as the influence of these noise sources on the test structure.

The measurements are carried out using a vector network analyzer. One input node ( $I$ ) is driven by the RF signal ( $V_I$ ) of the network analyzer, while the other ( $\bar{I}$ ) is terminated by  $50 \Omega$ . For this, a GSG ( $G_I S_I S_{\bar{I}} G_I$ ) configuration is used for the input probe. The supply voltage ( $V_0$ ) is also connected to the amplifier via an RF probe ( $G_0 S_0 G_0$ ). One node ( $Q$ ) of the differential amplifier output drives the test structure, while the other one ( $\bar{Q}$ ) is loaded by a dummy network. This network, which consists of

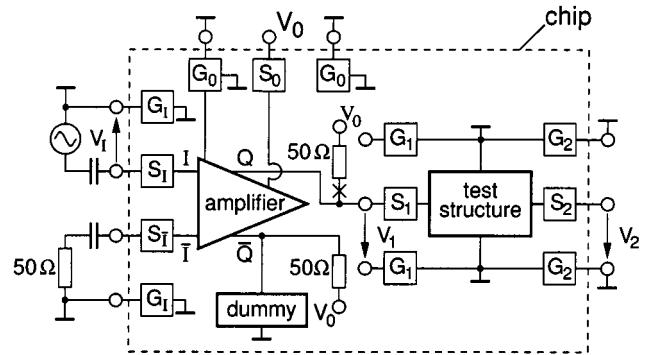


Fig. 4. Schematic of the measurement setup used to investigate very weak substrate coupling by utilizing a broad-band amplifier.

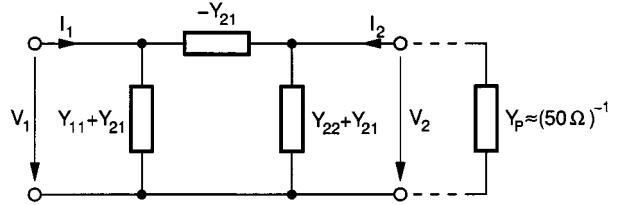


Fig. 5. Equivalent circuit of the test structure used to determine substrate coupling.  $Y_P$  is the input admittance of the RF probe.

several resistors and capacitors, models the (frequency-dependent) input impedance of the substrate test structure.<sup>2</sup> Thus, the output is loaded nearly symmetrically, further reducing the noise generated by the amplifier. The single-ended output of the test structure ( $V_2$ ) is connected to the input of the network analyzer via the probe  $G_2 S_2 G_2$ .

The substrate test structures discussed here can be described by the two-port equivalent circuit of Fig. 5, where  $Y_{21} = Y_{12}$  is assumed because of reciprocity. From this, the frequency-dependent complex transadmittance  $Y_{21}$ , which represents the substrate coupling under investigation, can be calculated as

$$Y_{21} = -(Y_{22} + Y_P) \cdot \frac{V_2}{V_1}. \quad (7)$$

For this, two unknowns have to be measured as shown below: the ratio of output and input voltage of the test structure  $V_2/V_1$ , as well as output admittance  $Y_{22}$  of the test structure.  $Y_P = (50 \Omega)^{-1}$  is the input admittance of the RF probe.

For the measurements described now, first an adequate level for the amplitude of the amplifier's input voltage  $V_I$  has to be chosen. It should be low enough to still guarantee linear operation of the output stage and also nearly linear behavior of the pn junctions of the test structure. On the other hand, the amplitude of  $V_I$  should be high enough to ensure that even at very weak substrate coupling the amplitude of the output signal  $V_2$  of the test structure lies well above the noise floor of the network analyzer. Then, in a first step,  $V_2/V_1$  is calculated from a measured set of  $S$ -parameters, which also yields the output admittance  $Y_{22}$  of the test structure. In a second step,  $V_1/V_I$  has to be determined in order to get the ratio  $V_2/V_1 = (V_2/V_I) \cdot (V_I/V_1)$

<sup>2</sup>The input impedance of the substrate test structure was estimated by substrate simulation. Subsequently, the element values of the dummy network were obtained by fitting [14], [17].

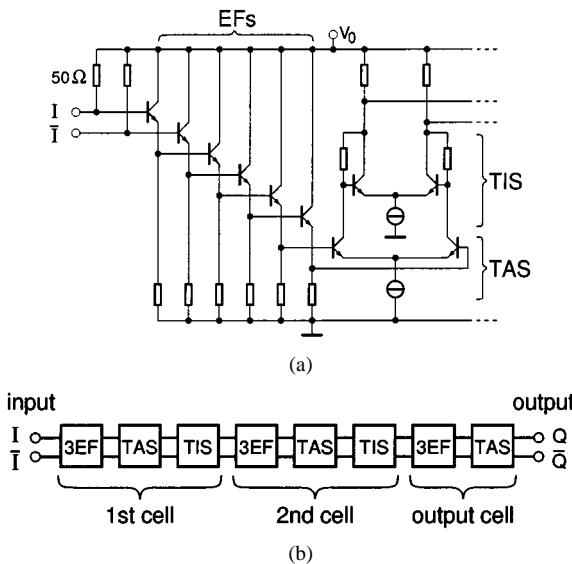


Fig. 6. Broad-band amplifier. (a) Simplified circuit diagram of the first cell. (b) Block diagram of the complete amplifier.

required to calculate  $Y_{21}$  from (7). For this, another set of S-parameters is measured, but now with the output probe positioned on the pads  $G_1 S_1 G_1$  and with the  $50\Omega$  load at the amplifier output node  $Q$  disconnected (by an ultrasonic cutter).<sup>3</sup>

### B. Circuit Diagram and Specifications of the Amplifier

The amplifier has to meet the following conditions:

- large bandwidth to cover a wide frequency range;
- high gain, so that the crosstalk between input and output probe can be neglected;
- output voltage swing high enough to get a sufficiently high signal amplitude at the input of the network analyzer (well above the noise floor) even for very weak substrate coupling;
- noise generated by the amplifier and fed into the test structure should be negligible (as discussed before).

To increase the bandwidth as far as possible, the principle of strong mismatching between succeeding (dc coupled) stages was applied [18]. Fig. 6(a) shows the circuit diagram of the first amplifier cell. It consists of three emitter follower (EF) pairs succeeded by a differential transadmittance stage (TAS) and transimpedance stage (TIS). The second amplifier cell looks very similar, but uses EFs in the feedback paths of the TIS and negative-feedback resistors  $R_E$  in series to the emitter of each TAS transistor. Moreover, the frequency response of its gain can be optimized by shunting an adjustable capacitor to the resistors  $R_E$ . The differential output cell, again, consists of three EF pairs and a TAS with negative-feedback resistors. The two output nodes are loaded on-chip by  $50\Omega$  resistors each and by the substrate test structure and its dummy, respectively. Fig. 6(b) shows the block diagram of the complete amplifier. The layout of the amplifier and the driven test structure are shown in Fig. 7.

The amplifier and test structure have been fabricated in a SiGe bipolar production technology of Atmel Germany GmbH, Heil-

<sup>3</sup>Instead, a second test configuration without  $50\Omega$  loading of the amplifier can be used. It should be arranged near the first one (on the same chip) to minimize the impact of fabrication spread.

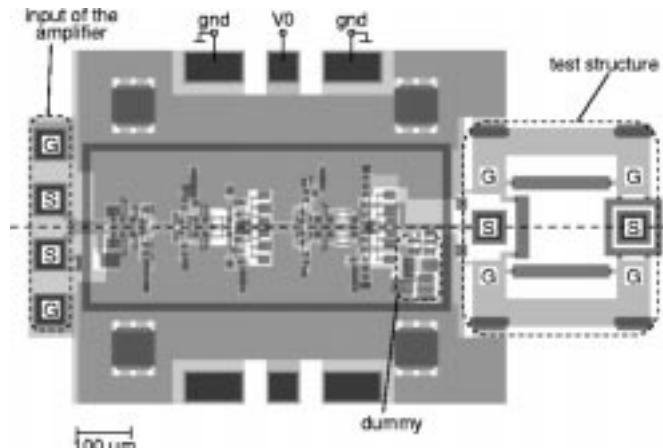


Fig. 7. Layout of the broad-band amplifier with connected test structure for substrate coupling. The total chip size is  $1.2 \times 0.6 \text{ mm}^2$ .

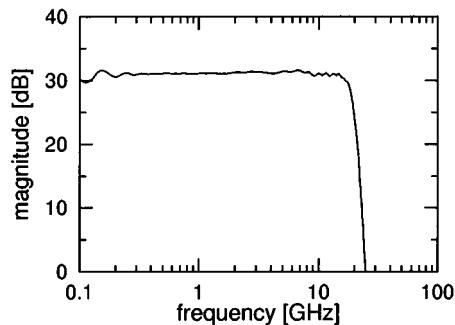


Fig. 8. Magnitude of the measured transfer function ( $S_{21}$ ) of the broad-band amplifier (loaded by the test structure for substrate coupling).

bronn. It is a self-aligned technology with a transistor transit frequency of 50 GHz and two metallization layers. The resistivity of the substrate is  $20 \Omega\text{-cm}$ , the sheet resistance of the channel stopper  $500 \Omega/\square$ , and the thickness of the wafer  $300 \mu\text{m}$ .

The measurement results agree well with the circuit simulation predictions. Fig. 8 shows the magnitude of the amplifier's transfer function  $S_{21}$  versus frequency with the output loaded by  $50\Omega$  (RF probe) and the test structure. The gain is 30 dB and nearly constant within the frequency range of interest. The 3-dB cutoff frequency is about 20 GHz. For linear operation, the maximum (single-ended) voltage swing at the output node  $Q$  is about 350 mV<sub>p-p</sub>.

### IV. COMPARISON OF THE TWO MEASUREMENT TECHNIQUES

The main advantage of the deembedding method is its very simple implementation, as it is sufficient to extend the contact pads for the RF probes by some connections and (optional) matching resistors. For utilizing the broad-band amplifier, significantly more design work has to be invested. However, once the amplifier has been developed for a given technology, it can be used to measure quite different substrate test structures.<sup>4</sup> As another advantage of the deembedding method, the maximum

<sup>4</sup>To optimally adjust the amplifier's transfer function and the impedance of the dummy network to the different loads caused by the investigated test structures, slight modifications are provided by changing circuit elements by (ultrasonic) cutting of metallization lines. However, this option is only required if the input impedances of the test structures differ substantially.

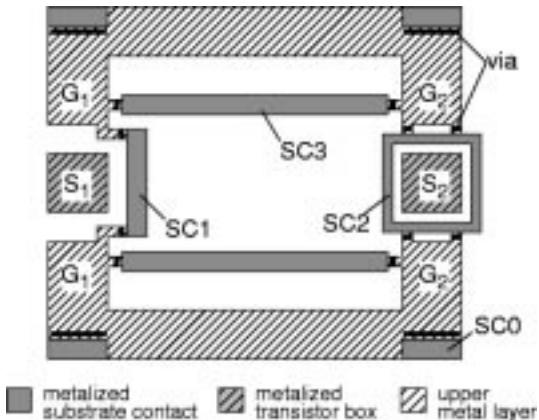


Fig. 9. Top view of a test structure for measuring very weak substrate coupling using the broad-band amplifier. The coupling path between two transistor isolation boxes ( $60 \times 60 \mu\text{m}$ ) over a long distance ( $300 \mu\text{m}$ ) is investigated. The amplifier (not shown here) is placed on the left side of the test structure (cf. Fig. 7).

measurement frequency is only limited by the measurement equipment. In contrast, the broad-band amplifier has an upper limiting frequency which depends on the technology used.

As a disadvantage of the deembedding method, at least five measurements are required to determine all error coefficients and the substrate coupling (cf. Section II). For all these measurements, crosstalk between the RF probes must be assumed to be unchanged. This assumption is not necessarily guaranteed due to slight variations in contact resistance and positioning of the probes. Consequently, special care is required to ensure a consistent set of measurement results. Furthermore, the achievable reduction of probe crosstalk is not reliably predictable and depends strongly on the dynamic range of the measurement system.

When using the amplifier method, only two measurements are required (cf. Section III). Moreover, the factor by which the probe crosstalk is reduced is known, as it is equal to the gain of the amplifier. Thus, it can be concluded that the results obtained with the amplifier method normally have a higher degree of accuracy for very weak substrate coupling since the probe crosstalk is reduced physically and the method is less sensitive to measurement uncertainties.

## V. TEST STRUCTURES FOR SUBSTRATE COUPLING

Several test structures have been designed and fabricated to investigate very weak substrate coupling and to verify the methods discussed in Sections II and III. An example, which is driven by the broad-band amplifier, is shown in Fig. 9. It consists of two transistor isolation boxes which have a size of  $60 \times 60 \mu\text{m}^2$  and are separated by  $300 \mu\text{m}$ .<sup>5</sup> Both boxes are connected to RF probe pads ( $S_1$  and  $S_2$ ) in the upper metallization layer. The left box is connected directly to the output of the amplifier and acts as a transmitter of substrate noise. Its bias voltage, which is given by the amplifier's output stage, is about 5.25 V, thus reducing the substrate capacitance of the box by a

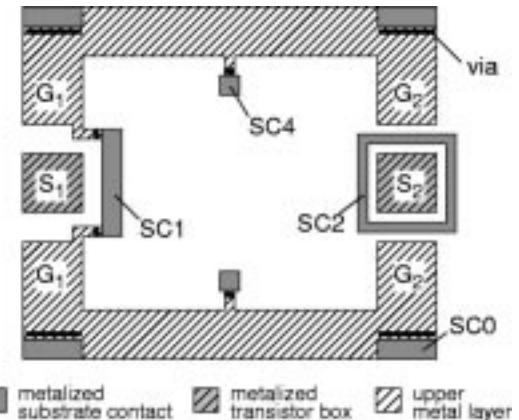


Fig. 10. Test structure with reduced shielding. Compared to Fig. 9, the substrate contacts parallel to the coupling path have been replaced by small square contacts, and the shield ring surrounding the receiving transistor isolation box has been deactivated by cutting its ground connections.

factor of 2.5 compared to the zero-biased case. This transmitter box is shielded by a rectangular substrate contact (SC1).

The transistor isolation box on the right side of the test structure (receiver) is zero-biased and is surrounded by a grounded substrate contact ring (SC2) with high shielding effectiveness. Additional substrate contacts are placed parallel to the coupling path (SC3) to further reduce coupling and, moreover, in the four corners of the test structure (SC0) to obtain a well-defined potential for the substrate surface (and the channel stopper), which is used as a reference ground for all measurements. The connections between all shielding substrate contacts and ground ( $G_1$ ,  $G_2$ ) have been designed to be as short as possible to minimize parasitic inductances which reduce the shielding effectiveness at high frequencies [15].

Another test structure with the same distance between transmitter and receiver box but reduced shielding, i.e., stronger coupling, is shown in Fig. 10. This test structure has small square substrate contacts (SC4) instead of the horizontal ones (SC3), and the shield ring of the receiving transistor isolation box has been deactivated by cutting its ground connections. Consequently, the shielding capability is reduced, and grounding of the channel stopper area between transmitter and receiver is not as good as before. The test structures in Figs. 9 and 10 can be directly driven by the broad-band amplifier. In order to be able to apply the deembedding procedure, short- and open-standards are required (cf. Section II). For this, the test structure of Fig. 9 is extended by the pad configuration of Fig. 2, as shown in Fig. 11.

Since the substrate coupling only between the two transistor isolation boxes is of interest, the influence of the pad capacitances and interconnection inductances has to be removed by an additional deembedding step. This is only possible if there is a well-defined ground beneath the probe pads ( $S_1, S_2$ ), which is provided here by grounded buried layer areas. These also help to reduce direct coupling of signals from the pads into the substrate. Apart from these extensions, the test structure equals that in Fig. 9, which is used in conjunction with the amplifier.

Additional test structures were designed and fabricated to measure the technological and electrical parameters required for

<sup>5</sup>This and the following test structures were also designed, and measured for shorter ( $200 \mu\text{m}$ ) and longer ( $400 \mu\text{m}$ ) distances. For additional test structures, see [15] and [17].

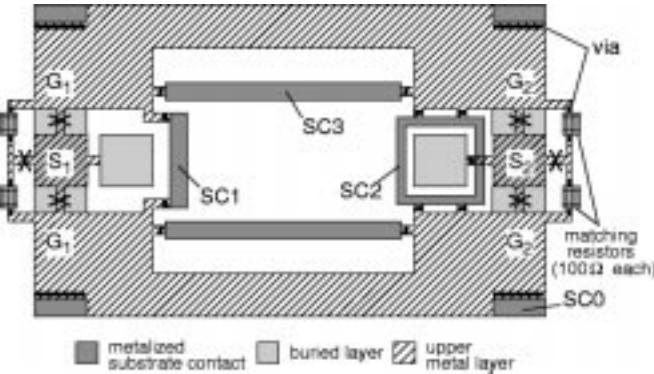


Fig. 11. Test structure used in conjunction with the deembedding method. The structure of Fig. 9 has been extended by the pad configuration of Fig. 2 so that the required standards can be fabricated by cutting interconnections with an ultrasonic cutter.

the numerical simulation [14]. These are, e.g., the sheet resistance of the channel stopper and inversion layer, the area-specific oxide capacitances between the metallization layers and the substrate, and the specific substrate capacitances of bottom and periphery of the transistor isolation boxes. These parameters were measured on the same wafer as the substrate coupling in order to avoid that the comparison between measurement and simulation is influenced by fabrication spread.

## VI. MEASUREMENT AND SIMULATION RESULTS

In this section, the results obtained with the two measurement techniques are presented and compared to the numerical substrate simulation. Again, coupling is defined by the transadmittance  $Y_{21}$  of the test structure. For the method using the amplifier,  $Y_{21}$  is easily obtained as described in Section III. For the deembedding technique, it can be obtained by converting the deembedded  $S$ -parameter set into a two-port admittance matrix and removing the influence of the pad capacitances and inductances of the interconnections between pads and transistor isolation boxes. For comparison, the admittance matrix is also calculated using the substrate simulator SUSI.

First, the results obtained with the broad-band amplifier are discussed. Fig. 12 shows the measured and simulated transadmittance for the test structure in Fig. 10 with reduced shielding. A very good agreement is observed for both magnitude and phase up to about 20 GHz, thus demonstrating the suitability of both the measurement method and the numerical simulator. The upper frequency limit is given by the cut-off frequency of the amplifier. The magnitude of the transadmittance at 10 GHz corresponds to a transimpedance of about 50 k $\Omega$  (corresponding to  $-60$  dB in a 50- $\Omega$  environment), which is remarkably high as only one of the two transistor isolation boxes is shielded. This is because the boxes are relatively small and the transmitting isolation box is strongly reverse-biased, thus having a reduced substrate capacitance.

By activating all shielding measures, as in the test structure of Fig. 9, substrate coupling is substantially reduced. The measurement and simulation results for this test structure are shown in Fig. 13. Compared to Fig. 12, substrate coupling is now reduced by an order of magnitude, resulting in a transimpedance as high as 0.5 M $\Omega$  (corresponding to  $-80$  dB in a 50- $\Omega$  system)

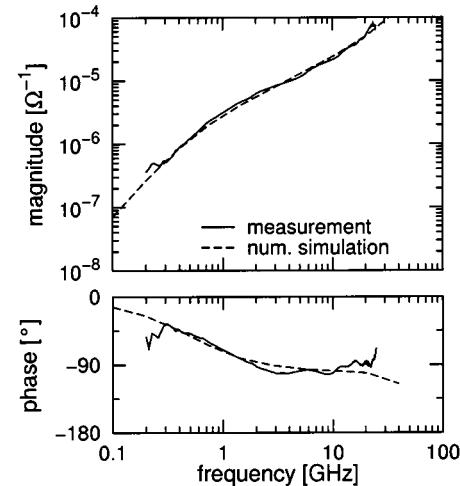


Fig. 12. Comparison of measured and simulated transadmittance  $Y_{21}$  for the test structure in Fig. 10 with reduced shielding. The measurement result was obtained with the broad-band amplifier.

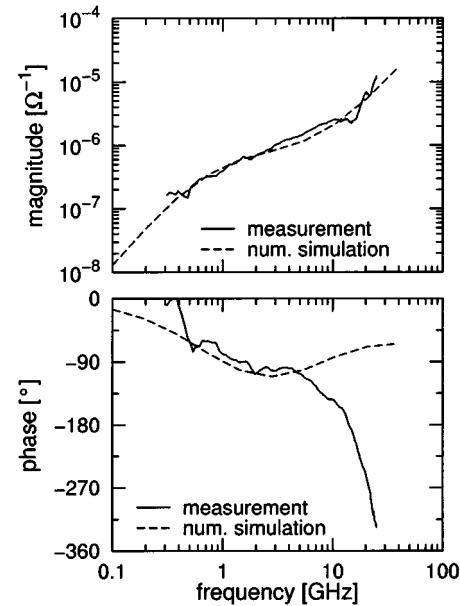


Fig. 13. Measured and simulated transadmittance  $Y_{21}$  for the test structure in Fig. 9 with weak coupling. The measurement result was obtained with the broad-band amplifier.

at 10 GHz. The good agreement of the magnitude of  $Y_{21}$  between measurement and simulation results at such a weak coupling demonstrates the suitability of both methods even under extreme conditions. However, the phase shows large deviations above 6 GHz. It is supposed that this is a result of the high sensitivity of the phase to the measurement environment, due to the very weak substrate coupling. This includes the influence of the metallic chuck, used to carry the chip or wafer during measurement, as well as the influence of adjacent structures on the same chip. Such effects are very difficult to describe and are, therefore, not considered in the substrate simulation.

In order to further reduce substrate coupling, the distance between the transistor isolation boxes in the test structure of Fig. 9 was increased from 300 to 400  $\mu\text{m}$ . In this case, transadmittances as low as  $2.7 \cdot 10^{-7} \Omega^{-1}$  (transimpedance 3.7 M $\Omega$ ) at

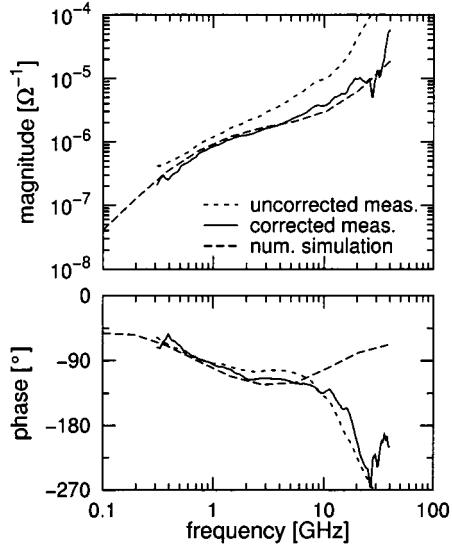


Fig. 14. Measured and simulated transadmittance  $Y_{21}$  for the extended test structure in Fig. 11. The measured transadmittance is shown with and without correction by the deembedding method.

1 GHz and  $1.3 \cdot 10^{-6} \Omega^{-1}$  (transimpedance  $0.77 \text{ M}\Omega$ ) at 10 GHz were measured, corresponding to  $-97$  and  $-84$  dB in a  $50\text{-}\Omega$  environment.

In addition, the method for deembedding the probe crosstalk was applied using the extended test structure of Fig. 11. The measurement results with and without deembedding of probe crosstalk are shown in Fig. 14. It is clearly demonstrated that the uncorrected data yields by far too high magnitudes of  $Y_{21}$ , here by up to a factor of 8 at 20 GHz. After deembedding, the magnitude of  $Y_{21}$  agrees quite well with the simulation result,<sup>6</sup> inserted for comparison, up to about 30 GHz. These results verify the deembedding of probe crosstalk under extreme conditions. However, above about 8 GHz larger deviations in the phase between the corrected measurement and simulation are observed. This may be caused by the dominating influence of probe crosstalk compared to the substrate coupling under investigation and by the influence of the environment of the test structure, as discussed before.

Additional test structures have been examined by applying the presented methods with both reduced and enlarged distances and also without channel stopper between the two transistor isolation boxes. Transimpedances of up to  $1 \text{ M}\Omega$  at 10 GHz were observed. For all structures, good agreement with the simulation results could be achieved.

The effectiveness of the different shielding measures, as applied in the test structures of Figs. 9 and 10, is now investigated and compared by numerical simulation with SUSI. The simulation results are shown in Fig. 15. Strong coupling is observed if the channel stopper between transmitter and receiver is grounded only via the substrate contacts SC0 (Fig. 10) in the corners of the test structure (curve 1). These contacts are also used in all of the following examples. The shielding effectiveness of this channel stopper layer is improved even by

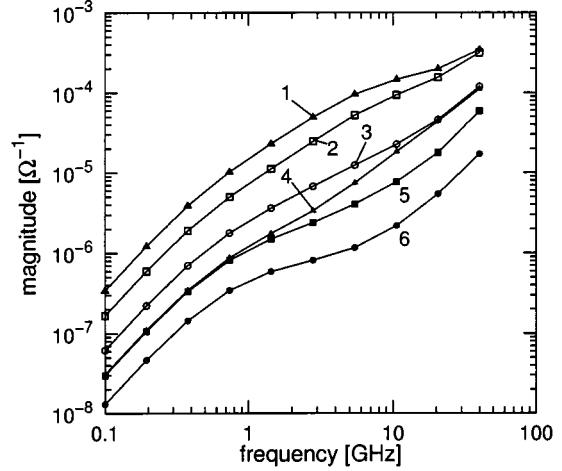


Fig. 15. Simulated transadmittances of the test structure in Figs. 9 and 10 for different degrees of shielding by substrate contacts (SC). (1) No shielding, only the four SCs in the corners are active (SC0). These contacts are also present in all the other cases. (2) Small square SCs in the center (SC4 in Fig. 10). (3) Vertical SC stripe at transmitter and small square SCs (SC1 and SC4 as in Fig. 10). (4) Horizontal SC stripes (SC3). (5) Shield ring at receiver and small square SCs (SC2 and SC4). (6) Transmitter and receiver shielded, horizontal SC stripes (SC1, SC2, and SC3 as in Fig. 9).

small square contacts SC4 (Fig. 10) near the main coupling path (curve 2).<sup>7</sup> If these contacts are lengthened over the whole distance between transmitter and receiver (SC3 in Fig. 9), coupling is substantially reduced (curve 4). Similar results are obtained at high frequencies if, instead of SC3 a vertical contact stripe SC1 (Fig. 9) is provided at the transmitter in addition to SC4 (curve 3); however, low-frequency shielding is worse. Shielding can be improved within the whole frequency range under investigation if instead of the vertical stripe at the transmitter a shield ring around the receiver is used (curve 5). Applying all shielding measures together, i.e., SC1, SC2, and SC3 as in Fig. 9, the magnitude of the transadmittance can be further reduced (curve 6), here down to  $4 \cdot 10^{-7} \Omega^{-1}$  (corresponding to  $2.5\text{-M}\Omega$  transimpedance) at 1 GHz and to  $2 \cdot 10^{-6} \Omega^{-1}$  (corresponding to  $0.5\text{-M}\Omega$  transimpedance) at 10 GHz.

## VII. CONCLUSION

Two methods have been presented and compared which allow the measurement of very weak substrate coupling up to high frequencies. Using shielded test structures, transadmittances as low as  $2.7 \cdot 10^{-7} \Omega^{-1}$  (transimpedance  $3.7 \text{ M}\Omega$ ) at 1 GHz and  $1.3 \cdot 10^{-6} \Omega^{-1}$  (transimpedance  $0.77 \text{ M}\Omega$ ) at 10 GHz could be measured, corresponding to  $-97$  and  $-84$  dB in a  $50\text{-}\Omega$  environment. The results of both measuring methods agree well with numerical simulations obtained by applying our substrate simulator SUSI. Thus, not only the measuring methods but also the suitability of SUSI are verified for very weak substrate coupling. As a consequence, SUSI proved again to be an efficient and flexible tool for investigating substrate coupling and adequate shielding methods in high-speed IC's.

It should be noted that the high effectiveness of the shielding methods investigated here can substantially deteriorate (espe-

<sup>6</sup>There is only a slight deviation from the simulation results in Fig. 13 which is mainly caused by the additional shielding of the transmitting and receiving transistor isolation boxes due to the influence of the buried layer beneath the pads  $S_1$  and  $S_2$ .

<sup>7</sup>Without channel stopper (but considering the resulting inversion layer) similar results are obtained up to about 2 GHz, but weaker coupling is observed at higher frequencies.

cially at high frequencies [15]) if the grounding of the shields is worse compared to the examples presented here. This is the case if, e.g., parasitic inductances caused by on-chip wiring, bonds, or package leads are located between shield and ground. The influence of these inductances may be reduced if the backside of the chip acts as a shield. For this, several preconditions have to be met. For example, the substrate must be thinner than the distance between transmitter and receiver, and the backside of the chip must be carefully grounded. If there is a certain parasitic inductance between backside and ground, coupling can even increase.

All these effects have been considered in practical designs. For this the numerical simulation results calculated by SUSI were converted into an equivalent substrate network with few lumped elements [15], [19], which can easily be handled in a circuit simulator such as SPICE, together with all additional parasitics.

## REFERENCES

- [1] K. J. Kerns, I. L. Wemple, and A. T. Yang, "Efficient parasitic substrate modeling for monolithic mixed-A/D circuit design and verification," in *Analog Integrated Circuits and Signal Processing*. Norwell, MA: Kluwer, 1996, vol. 10, pp. 7-21.
- [2] N. K. Verghese and D. J. Allstot, "Computer-aided design considerations for mixed-signal coupling in RF integrated circuits," *IEEE J. Solid-State Circuits*, vol. 33, pp. 314-323, Mar. 1998.
- [3] J. Briaire and K. S. Kirsch, "Principles of substrate crosstalk generation in CMOS circuits," *IEEE Trans. Computer-Aided Design*, vol. 19, pp. 645-653, June 2000.
- [4] X. Aragonès and A. Rubio, "Experimental comparison of substrate noise coupling using different wafer types," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1405-1409, Oct. 1999.
- [5] T. Blalack, J. Lau, F. J. R. Clément, and B. A. Wooley, "Experimental results and modeling of noise coupling in a lightly doped substrate," in *Proc. IEEE IEDM*, Dec. 1996, pp. 623-626.
- [6] D. K. Su, M. J. Loinaz, S. Masui, and B. A. Wooley, "Experimental results and modeling techniques for substrate noise and mixed-signal integrated circuits," *IEEE J. Solid-State Circuits*, vol. 28, pp. 420-430, Apr. 1993.
- [7] R. Gharpurey and R. G. Meyer, "Modeling and analysis of substrate coupling in integrated circuits," in *Proc. IEEE CICC*, 1998, pp. 487-490.
- [8] J. M. Casalta, X. Aragonés, and A. Rubio, "Substrate coupling evaluation in BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 32, pp. 598-603, Apr. 1997.
- [9] M. v. Heijningen, J. Compie, P. Wambacq, S. Donnay, M. G. E. Engels, and I. Bolsens, "Analysis and experimental verification of digital substrate noise generation for epi-type substrates," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1002-1008, July 2000.
- [10] A. Samavedam, A. Sadate, K. Mayaram, and T. S. Fiez, "A scalable substrate noise coupling model for design of mixed-signal IC's," *IEEE J. Solid-State Circuits*, vol. 35, pp. 895-904, June 2000.
- [11] K. Joardar, "Signal isolation in BiCMOS mixed mode integrated circuits," in *Proc. IEEE BCTM*, 1995, pp. 178-181.
- [12] J.-P. Raskin, A. Viviani, D. Flandre, and J.-P. Colinge, "Substrate crosstalk reduction using SOI technology," *IEEE Trans. Electron Devices*, vol. 44, pp. 2252-2261, Dec. 1997.
- [13] J. S. Hamel, S. Stefanou, M. Bain, B. M. Armstrong, and H. S. Gamble, "Substrate crosstalk suppression capability of silicon-on-insulator substrates with buried ground planes (GPOI)," *IEEE Microwave Guided Wave Lett.*, vol. 10, pp. 134-135, Apr. 2000.
- [14] M. Pfost, H.-M. Rein, and T. Holzwarth, "Modeling substrate effects in the design of high-speed Si-bipolar IC's," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1493-1501, Oct. 1996.
- [15] M. Pfost and H.-M. Rein, "Modeling and measurement of substrate coupling in Si-bipolar IC's up to 40 GHz," *IEEE J. Solid-State Circuits*, vol. 33, pp. 582-591, Apr. 1998.
- [16] H. Heuermann and B. Schiek, "Robust algorithms for Txx network analyzer self-calibration procedures," *IEEE Trans. Instrum. Meas.*, vol. 43, pp. 18-23, Feb. 1994.
- [17] M. Pfost, H.-M. Rein, W. Steiner, and A. Stürmer, "Simulation of substrate coupling with special regard to shielding in high-speed Si/SiGe bipolar ICs," in *Proc. Eur. Microwave Conf.*, 1999, pp. 133-136.
- [18] H.-M. Rein and M. Möller, "Design considerations for very-high-speed Si-bipolar IC's operating up to 50 Gb/s," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1076-1090, Aug. 1996.
- [19] M. Pfost, "Modeling of the substrate in high-speed silicon bipolar integrated circuits," Dr.-Ing. dissertation (in German), Ruhr-Universität Bochum, Bochum, Germany, Apr. 2000.



**Wolfgang Steiner** was born in Essen, Germany, in 1974. He received the Dipl.-Ing. degree in electrical engineering from the Ruhr-University Bochum, Bochum, Germany, in 1998.

He then joined the Institute of Electronics (Arbeitsgruppe Halbleiterbauelemente) at the Ruhr-University Bochum as a Research Assistant. His main field of research is simulation and modeling of parasitic substrate effects in high-speed bipolar ICs.



**Martin Pfost** (S'91-M'00) received the Dipl.-Ing. and Dr.-Ing. degrees in electrical engineering from the Ruhr-University Bochum, Bochum, Germany, in 1993 and 2000, respectively.

From 1993 to 1998, he was with the Institute of Electronics, Ruhr-University Bochum, as a Research Assistant, where he was involved in the simulation and modeling of parasitic substrate effects in high-speed bipolar ICs. Since 1999, he has been with Infineon Technologies AG, Munich, Germany, working on GaAs HBT ICs for portable telephone

applications. His current research interests include power amplifier design, RF measurement techniques, numerical temperature simulation, and microwave device modeling.



**Hans-Martin Rein** (M'92-SM'99-F'01) received the Dipl.-Ing. and Dr.-Ing. degrees in electrical engineering from the University of Stuttgart, Stuttgart, Germany, in 1964 and 1968, respectively.

From 1968 to 1973, he was with the Semiconductor Division, AEG-Telefunken, Heilbronn, Germany. As Head of a department, he was responsible for the development of high-speed bipolar circuit families and of advanced MOS/CMOS technologies. Since 1973, he has been a Professor at Ruhr-University Bochum, Bochum, Germany, where he teaches ICs. His main fields of research are the design and optimization of high-speed analog and digital Si-bipolar ICs (especially for optical communications and microwave applications) with operating speeds up to 60 GHz and 60 Gb/s, respectively, as well as modeling of very fast bipolar transistors (including SiGe HBTs) and on-chip parasitics (e.g., substrate coupling). He has authored or co-authored approximately 150 technical papers and a textbook on integrated bipolar circuits.



**Anton Stürmer** received the Diploma in physics from the University of Würzburg, Würzburg, Germany, in 1969.

From 1969 to 1981, he was with the AEG-Telefunken Research Institute, Ulm, Germany, where he was involved with the development of technological processes. He then joined the Design Center of Integrated Circuits, AEG, where he was involved with the modeling of semiconductor devices and IC measurement. He is currently with Atmel Germany GmbH (formerly TEMIC Semiconductor GmbH), Ulm, Germany, where he is a member of the CAD Group. His main fields of work are parasitic effects and reuse of design knowledge in analog ICs.



**Andreas Schüppen** was born in Geilenkirchen, Germany, in 1961. He received the Dipl.-Ing. and Ph.D. degrees from the RWTH Aachen, Aachen, Germany, in 1988 and 1993, respectively.

From 1988, he was a Research Assistant with the Institute of Thin Film and Ion Technology, Research Center, Jülich, Germany, where he was involved with silicon permeable base transistors. In 1993, he joined the Daimler Benz Research Center, Ulm, Germany, where he was responsible for the SiGe-technology transfer to TEMIC Semiconductors, Heilbronn, Germany. From 1994 to 1996, he was member of the Daimler Benz "Austauschgruppe," a special group for junior scientists. Since 1996, he has been a Project Manager of SiGe at TEMIC Semiconductors, which was taken over by ATMEL in 1998.

Dr. Schüppen was the recipient of the 1993 European Material Research Society Young Scientist Award and the 1995 Cooperation Award Science-Economy of the University of Ulm.